REMARKS

The Office Action dated February 26, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1 and 5 have been amended, and claim 2 has been cancelled without prejudice. New claims 6-7 have been added. Applicants submit that the new claims as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1 and 3-7 are pending in the present application and are respectfully submitted for consideration.

Error Made in the Notice of References Cited (PTO-892)

Applicants respectfully request the correction of an error made in the Notice of References Cited (PTO-892) and requesting the issuance of a corrected copy of the Notice of References Cited, and that the correction to be of record in the file history of the application.

The Office Action mailed September 23, 2004 rejected claim 2 under 35 U.S.C. §103(a) as being unpatentable over Heuner et al. (US Patent No. 4,066,918) in view of McDaniel (US Patent No. 5,243,236), among other things. The rejection of claim 2 as noted in the "Detailed Action" portion of the Office Action correctly cites the reference of McDaniel as "(5,243,236)." There appears to be no errors regarding the citation of the references in the "Detailed Action." However, the Notice of References Cited (PTO-892) accompanying the Office Action listed reference "B" as "US-243,236" to McDaniel.

It is submitted that an error was made regarding the citation of the document number concerning McDaniel. The correct citation should be --US-5,243,236--.

Section 707.05(g) of the MPEP also states that,

> Where an error in citation of a reference is brought to the attention of the Office by applicant, a letter correcting the error, together with a correct copy of the reference, is sent to applicant. ... [t]The examiner is directed to correct the error, in ink, in the paper in which the error appears, and place his or her initials on the margin of such paper, together with a notation of the paper number of the action in which the citation has been correctly given.

Therefore, Applicants respectfully request that the Examiner issue a new Notice of Reference Cited correcting the error. Applicants further recommend request that the Examiner correct the error in ink in the attached copy of Notice of Reference Cited, and place his initials on the margin of the paper and provide a copy of the same to the Applicants.

Formal Matters

The title of the invention was not descriptive. Applicants respectfully submit a more descriptive new title of -- SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE CONFIGURED TO PREVENT THE GENERATION OF A REVERSE CURRENT IN A MOS TRANSISTOR -- for consideration.

Claims 1 and 3-5 Recite Patentable Subject Matter

Claims 1 and 3 were rejected under 35 U.S.C. § 102(b) as being anticipated by Heuner et al. (U.S. Patent No. 4,066,918, "Heuner"). Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a semiconductor integrated circuit device comprising, among other features, a second MOS transistor, of a same conductivity type as the first MOS transistor, wherein a load is connected to a connecting portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor, and wherein, between the first backgate region and the second conducting region of the first MOS transistor, a first parasitic diode is formed and, between the second backgate region and the fourth conducting region of the second MOS transistor, a second parasitic diode is formed.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

The Office Action characterized Heuner as allegedly disclosing "a first MOS transistor N1 having a first backgate region 305, a first conductive region 233, and a second conductive region 235, and having the first backgate region and the first conductive region thereof connected together; a second MOS transistor P1 having a second backgate region 330, a third conductive region 221, and a fourth conductive region 223 ..."

Applicants submit that Heuner fails to disclose or suggest each and every element recited in claims 1 of the present application. In particular, it is submitted that the elements D_{P1}, D_{P2} and D_{N1}, D_{N2} of Heuner are neither comparable nor analogous to the parasitic diodes of the present invention.

For example, in the first MOS transistor of the present invention, the first backgate and the second conductive region together from the parasitic diode Dx2; and

in the second MOS transistor of the present invention, the second backgate and the fourth conducting region together from the parasitic diode Dx1. The present invention provides the advantage of preventing a reverse current with these parasitic diodes Dx1 and Dx2 and to exploit the low on-state resistance of the first MOS transistor to reduce the voltage drop across it.

In contrast, the elements D_{P1} and D_{P2} of Heuner are formed between the source and drain, respectively, of the P-channel MOS transistor P1 and the substrate; and the elements D_{N1} and D_{N2} are formed between the source and drain, respectively, of the N-channel MOS transistor N1 and the N-type substrate 213. With these elements of Heuner, however, a reverse current cannot be prevented. Thus, Applicants submit that Heuner fails to disclose or suggest each and every element recited in claim 1 of the present application, and therefore is allowable.

As claim 3 depends from claim 1, Applicants submit that claim 3 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Heuner fails to disclose or suggest each and every feature of claims 1 and 3. Accordingly, Applicants respectfully submit that claims 1 and 3 are not anticipated by nor rendered obvious by the disclosure of Heuner. Therefore, Applicants respectfully submit that claims 1 and 3 are also allowable.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Heuner in view of McDaniel (U.S. Patent No. 5,243,236, "McDaniel"). Claim 2 has been canceled without prejudice, and therefore the rejection is now moot.

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Heuner in view of Stewart (U.S. Patent No. 3,967,295, "Stewart"). Applicants respectfully traverse the rejection.

Heuner is discussed above.

Stewart is applied for allegedly teaching "a voltage setting circuit being composed of voltage division resistors." Stewart does not overcome the above-described drawback of Heuner as Stewart does not teach or suggest at least a second MOS transistor, of a same conductivity type as the first MOS transistor, wherein a load is connected to a connecting portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor, and wherein, between the first backgate region and the second conducting region of the first MOS transistor, a first parasitic diode is formed and, between the second backgate region and the fourth conducting region of the second MOS transistor, a second parasitic diode is formed.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Heuner and Stewart, alone or in combination, do not teach or suggest each feature recited by pending Claim 4.

Accordingly, for the above provided reasons, Applicants respectfully submit that pending Claim 4 is not rendered obvious under 35 U.S.C. § 103 by the teachings of Heuner and Stewart. Furthermore, Applicants respectfully note that Claim 4 depends from Claim 1. Therefore, it is respectfully submitted that Claim 4 should be deemed allowable for at least the same reasons Claim 1 is allowable, as well as for the additional subject matter recited therein.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Heuner and McDaniel, and further in view of Stewart. Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 5 recites a semiconductor integrated circuit device comprising, among other features, wherein a load is connected to a connecting portion between the first P-type diffusion layer of the first MOS transistor and the third P-type diffusion layer of the second MOS transistor, and wherein, between the first backgate and the second P-type diffusion layer of the first MOS transistor, a first parasitic diode is formed and, between the second backgate and the fourth P-type diffusion layer of the second MOS transistor, a second parasitic diode is formed.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Heuner is discussed above.

McDaniel is cited for allegedly teaching "first and second MOS transistors having the same polarity," and Stewart is applied for allegedly teaching "a voltage setting circuit having one end thereof grounded."

It is submitted that McDaniel and Stewart do not overcome the above-described drawback of Heuner as McDaniel and/or Stewart do not teach or suggest at least wherein a load is connected to a connecting portion between the first P-type diffusion layer of the first MOS transistor and the third P-type diffusion layer of the second MOS transistor, and wherein, between the first backgate and the second P-type diffusion layer of the first MOS transistor, a first parasitic diode is formed and, between the second backgate and the fourth P-type diffusion layer of the second MOS transistor, a second parasitic diode is formed.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Heuner, McDaniel and Stewart, alone or in combination, do not teach or suggest each feature recited by pending Claim 5. Accordingly, for the above provided reasons, Applicants respectfully submit that pending Claim 5 is not rendered obvious under 35 U.S.C. § 103 by the teachings of Heuner, McDaniel and Stewart, and therefore is allowable.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103,

there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action restates the advantages of the present invention to justify the combination of references. There is, however, nothing in the applied references to evidence the desirability of these advantages in the disclosed structure.

Applicants respectfully request withdrawal of the rejection.

New Claims 6 and 7 Recite Patentable Subject Matter

As claims 6 and 7 depend from claim 5, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1 and 3-7 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1 and 3-7 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 103213-00072.

Respectfully submitted,

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SH:grs
Enclosure: Copy of Notice of References Cited (PTO-892)